STACKED MEMORY CELL AND PROCESS OF FABRICATING SAME

RELATED APPLICATIONS

This application is a continuation-in-part application under 37 CFR 1.53(b) of co-pending U.S. Patent Application Serial No. 09/998,469 filed November 29, 2001, which is hereby incorporated by reference.

FIELD OF THE INVENTION

The invention relates in general to the structure and fabrication of integrated circuits and more particularly to an integrated circuit providing effective protection of selected circuit components, such as transistors and ferroelectric materials, against diffusion of oxygen and hydrogen.

BACKGROUND OF THE INVENTION

Ferroelectric compounds possess favorable characteristics for use in nonvolatile integrated circuit memories. See U.S. Patent No. 5,046,043 issued September 3, 1991 to Miller et al. A ferroelectric device, such as a capacitor, is useful as a nonvolatile memory when it possesses desired electronic characteristics, such as high residual polarization, good coercive field, high fatigue resistance, and low leakage current. Lead-containing ABO_3-type ferroelectric oxides such as PZT (lead zirconium titanate) and PLZT (lead lanthanum zirconium titanate) have been studied for practical use in integrated circuits. Layered superlattice material oxides have also been studied for use in integrated circuits. See U.S. Patent No. 5,434,102 issued July 18, 1995 to Watanabe et al. Layered superlattice materials exhibit characteristics in ferroelectric memories that generally are superior to those of PZT and PLZT compounds. Integrated circuit devices containing ferroelectric elements are currently being manufactured. Nevertheless, problems associated with oxygen degradation and hydrogen degradation during the manufacturing process hinders the economical production in commercial quantities of ferroelectric memories and other IC devices using either the ABO_3-type oxides or the layered superlattice material compounds with the desired electronic characteristics.

A typical memory in an integrated circuit contains a semiconductor substrate and a metal-oxide semiconductor field-effect transistor (MOSFET)

electrically connected to a capacitor device. Layered superlattice materials and other dielectric capacitor materials currently in use and development comprise metal oxides. In conventional fabrication methods, crystallization of the metal oxides to produce desired electronic properties requires heat treatments in oxygen-containing gas at elevated temperatures. The heating in the presence of oxygen is typically performed at a temperature in a range of 500°C to 900°C for 60 minutes to three hours. As a result of the presence of reactive oxygen at elevated temperatures, numerous defects, such as dangling bonds, are generated in the single crystal structure of the semiconductor silicon substrate, leading to deterioration in the electronic characteristics of the MOSFET. Good ferroelectric properties have been achieved in the prior art using process heating temperatures at about 700°C to crystallize layered superlattice material. See U.S. Patent No. 5,508,226, issued April 16, 1996 to Ito et al. Nevertheless, the long exposure times for up to several hours in oxygen, even at the somewhat reduced temperature ranges, results in oxygen damage to the semiconductor substrate and other elements of a CMOS circuit.

After completion of the integrated circuit, the presence of oxides may still cause problems because oxygen atoms from a thin film of metal oxide capacitor dielectric, for example, from ferroelectric layered superlattice material, tend to diffuse through the various materials contained in the integrated circuit and combine with atoms in the integrated circuit substrate and in semiconductor layers forming undesired oxides. The resulting oxides interfere with the function of the integrated circuit; for example, they may act as dielectrics in the semiconducting regions, thereby forming virtual capacitors. Diffusion of atoms from the underlying semiconductor substrate and other circuit layers into the ferroelectric metal oxide (or other dielectric metal oxide) is also a problem; for example, silicon from a silicon substrate and from polycrystalline silicon contact layers is known to diffuse into layered superlattice material and degrade its ferroelectric properties. For relatively low-density applications, the ferroelectric memory capacitor is placed on the side of the underlying CMOS circuit, and this may reduce somewhat the problem of undesirable diffusion of atoms between circuit elements. Nevertheless, as the market demand and the technological ability to manufacture high-density

circuits increase, the distance between circuit elements decreases, and the problem of molecular and atomic diffusion between elements becomes more acute. To achieve high circuit density by reducing circuit area, the capacitor of a memory cell is placed virtually on top of the switch element, typically a field-effect transistor ("MOSFET"), and the switch and bottom electrode of the capacitor are electrically connected by an electrically conductive plug. To inhibit undesired oxygen diffusion, a barrier layer is sometimes disposed under the ferroelectric or other dielectric oxide, between the capacitor's bottom electrode and the underlying layers. The barrier layer must inhibit the diffusion of oxygen and other chemical species that may cause problems; it must also be electrically conductive, to enable electrical connection between the capacitor and the switch. Such barrier layers are typically limited in size to cover only the surface area of an integrated circuit substrate located approximately directly below the capacitor.

To restore the silicon properties of the MOSFET/CMOS, the manufacturing process typically includes a forming-gas, or hydrogen, annealing ("FGA") process, in which defects such as dangling bonds are eliminated by utilizing the reducing property of hydrogen. Various techniques have been developed to effect the hydrogen annealing, such as H_2-gas heat treatment in ambient conditions. Conventionally, hydrogen treatments are conducted between 350°C and 550°C, typically around 400°C to 450°C for a time period of about 30 minutes. In addition, the CMOS/MOSFET manufacturing process requires other fabrication processes that expose the integrated circuit to hydrogen, often at elevated temperatures, such as hydrogen-rich plasma CVD processes for depositing metals and dielectrics, growth of silicon dioxide from silane or TEOS sources, and etching processes using hydrogen and hydrogen plasma. During processes that involve hydrogen, the hydrogen diffuses through the top electrode and the side of the capacitor to the thin film of metal-oxide capacitor dielectric (e.g., ferroelectric layered superlattice material) and reduces the oxides contained in the dielectric material. The absorbed hydrogen also metallizes the surface of the dielectric thin film by reducing metal oxides. The adhesivity of the dielectric thin film to the upper electrode is lowered by the chemical change taking place at the interface. Alternatively, the upper electrode is pushed up by the oxygen gas, water, and

other products of the oxidation-reduction reactions taking place. As a result of these effects, the electronic properties of the capacitor are degraded, and peeling is likely to take place at the interface between the top electrode and the dielectric thin film. In addition, hydrogen also can reach the lower electrode, leading to internal stresses that cause the capacitor to peel off its substrate. These problems are acute in ferroelectric memories containing layered superlattice material compounds because these metal oxide compounds are particularly complex and prone to degradation by hydrogen-reduction. After a forming-gas anneal (FGA), the remanent polarization of the ferroelectrics typically is very low and no longer suitable for storing information. Also, an increase in leakage currents results.

Several methods have been reported in the art to inhibit or reverse hydrogen degradation of desired electronic properties in ferroelectric oxide materials. Oxygen annealing at high temperature (800°C) for about one hour results in virtually complete recovery of the ferroelectric properties degraded by hydrogen treatments. However, the high-temperature oxygen anneal itself may generate defects in silicon crystalline structure, and it may offset somewhat the positive effects of any prior forming-gas anneal on the CMOS characteristics. Special metallization layers and diffusion barrier layers have also been examined to minimize the effects of hydrogen during high-energy processes and forming-gas annealing processes. The metallization schemes typically involve the use of materials that are prone to oxidation in an oxygen-containing environment at temperatures above 400°C. Aluminum, the primary metallization material, has a low melting point and cannot tolerate temperatures above 450°C. Thus, oxygen annealing of an integrated circuit substrate to repair prior hydrogen degradation is often not practically possible. Encapsulation of metal-oxide capacitor dielectric with hydrogen-diffusion barriers has been proposed in the prior art; nevertheless, it is often not completely effective, and it typically requires complex process schemes including depositing and removing the hydrogen barrier material.

SUMMARY OF THE INVENTION

Structures and methods in accordance with the invention provide integrated circuits that avoid the degradation of electronic properties resulting from undesired diffusion of oxygen and hydrogen within an integrated circuit, especially within

ferroelectric memory cells, but which do not add substantial changes to conventional CMOS processing or introduce complicated process schemes.

In one aspect, an embodiment in accordance with the invention provides an integrated circuit comprising: a switch; a capacitor; and an electrically nonconductive buried diffusion barrier located between the switch and the capacitor, the buried diffusion barrier substantially covering the switch. Preferably, the buried diffusion barrier comprises silicon nitride. Preferably, the integrated circuit further comprises an electrically conductive oxygen-diffusion barrier located between the buried diffusion barrier and the capacitor, the capacitor located on the conductive oxygen-diffusion barrier, wherein the nonconductive buried diffusion barrier and the conductive oxygen-diffusion barrier together continuously cover the switch. Preferably, the electrically conductive oxygen-diffusion barrier comprises titanium aluminum nitride, iridium, and iridium oxide. Preferably, the integrated circuit further comprises an electrically nonconductive hydrogen-diffusion barrier layer continuously covering the capacitor and the switch. Preferably, the nonconductive hydrogen-diffusion barrier comprises strontium tantalate. Preferably, the integrated circuit further comprises: an electrically conductive plug, the conductive plug located between the switch and the conductive diffusion barrier, the conductive plug having a bottom end and a top end; the bottom end being in electrical contact with the switch, and the top end being in electrical contact with the conductive oxygen-diffusion barrier. Preferably, the conductive plug comprises tungsten, titanium, and titanium nitride. Preferably, the capacitor comprises: a bottom electrode located on the conductive diffusion barrier; a dielectric thin film located on the bottom electrode; a top stack-electrode located on the dielectric thin film; and a top plate-line electrode, a portion of the top plate-line electrode being located on the top stack-electrode, the top plate-line electrode defining a plate-line axis; wherein the conductive diffusion barrier, the bottom electrode, the dielectric thin film, and the top stack-electrode are included in a self-aligned capacitor stack located on a capacitor portion of the second insulator layer. Preferably the capacitor stack has an insulated sidewall substantially perpendicular to the plate-line axis, and wherein the capacitor stack has a protected sidewall substantially parallel to the plate-line axis. Preferably, the integrated circuit further

comprises an insulator layer, a portion of which covers the insulated sidewall. Preferably, the integrated circuit further comprises: an electrically nonconductive hydrogen-diffusion barrier layer continuously covering the capacitor and the switch, and the nonconductive hydrogen-diffusion barrier comprises a plate-line portion covering a top plate-line electrode, a sidewall portion covering the protected sidewall, and a switch-portion located on the switch portion of the buried diffusion barrier. Preferably, the nonconductive hydrogen-diffusion barrier does not cover a nonmemory area of the integrated circuit. Preferably, the top plate-line electrode is wider than the capacitor stack in an orientation parallel to the plate-line axis. Preferably, the integrated circuit further comprises a plate-line connector located remotely from the capacitor stack. Preferably, the integrated circuit further comprises a bit-line plug, the bit-line plug comprising a bottom end and a top end, the bottom end in electrical contact with the switch, and the top end in electrical contact with a wiring layer. Preferably, the dielectric thin film comprises a ferroelectric layered superlattice material. Preferably, the thin film has a thickness not exceeding 90 nm.

In still another aspect, the invention also provides a method of fabricating an integrated circuit comprising: providing a substrate, the substrate comprising a switch and a capacitor stack, the capacitor stack comprising a top stack-electrode, a thin film of capacitor dielectric, a bottom electrode, and a conductive diffusion barrier, the conductive oxygen-diffusion barrier located above the switch; forming a top plate-line electrode on the top stack-electrode; and forming a continuous electrically nonconductive hydrogen-diffusion barrier layer on the plate-line electrode, on the capacitor stack, and on a switch area of the substrate.

In yet another aspect, the invention provides a method of fabricating a ferroelectric integrated circuit comprising: providing a substrate; forming a stack of capacitor layers over the substrate, the stack including a bottom electrode layer, a thin film capacitor ferroelectric layer, and a top stack-electrode layer; removing portions of the top stack-electrode layer, the ferroelectric thin film, and the bottom electrode layer, thereby forming a plurality of separated capacitor stacks, each comprising a top stack-electrode, a ferroelectric thin film, and a bottom electrode; forming a capacitor insulator layer over the capacitor stacks, filling in the removed

portions and thereby insulating the capacitor stacks from one another and protecting their sides; removing a portion of the capacitor insulator layer from at least a contact portion of the top surface of the top stack-electrodes; and thereafter forming a top plate-line electrode layer on the contact portion of the top stack-electrode and on the capacitor insulator layer. Preferably, providing a substrate comprises: providing a substrate including a switch and a first insulator layer covering the switch; forming a conductive plug through the first insulator layer, with a bottom end and a top end, the bottom end in electrical contact with the switch; and planarizing the top end of the conductive plug; and the capacitor stack is formed over the conductive plug. Preferably, the forming a stack of capacitor layers further comprises forming a conductive oxygen-diffusion barrier layer prior to forming the bottom electrode layer, and the removing portions of the top stack-electrode layer includes removing portions of the conductive oxygen-diffusion barrier layer. Preferably, the removing portions of the top stack-electrode layer comprises: depositing a hardmask on the top stack-electrode; patterning the hardmask; etching the top stack-electrode layer, the ferroelectric thin film, and the bottom electrode layer; removing the hard mask; and etching the barrier layer. Preferably, the top-stack electrode layer is from 5 nm to 100 nm thick. Preferably, the top-stack electrode layer is 50 nm thick. Preferably, the removing a portion of the capacitor insulator layer comprises planarizing the capacitor insulator layer to expose the top stack-electrodes. Preferably, the method further includes crystallizing the ferroelectric layer prior to the removing portions of the top stack-electrode layer, the ferroelectric thin film, and the bottom electrode layer. Alternatively, the method includes crystallizing the ferroelectric layer after the removing portions of the top stack-electrode layer, the ferroelectric thin film, and the bottom electrode layer.

The invention not only provides for better protection and isolation of the ferroelectric and MOS portions of the integrated circuit, but does so while reducing the complexity of the fabrication process. Numerous other features, objects and advantages of the invention will become apparent from the following description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 depicts a flow sheet of a method in accordance with the invention for making a preferred embodiment of a ferroelectric memory in accordance with the invention;

FIG. 2 depicts an integrated circuit substrate in accordance with the invention containing silicon semiconductor material, field oxide regions, and switches ("MOSFETs");

FIG. 3 depicts an electrically nonconductive "buried" diffusion barrier layer in accordance with the invention formed on a first insulator layer of the substrate depicted in FIG. 2;

FIG. 4 depicts a second insulator layer in accordance with the invention formed on the buried diffusion barrier layer shown in FIG. 3;

FIGS. 5 and 5A depict sections in which the substrate shown in FIG. 4 has been etched in accordance with the invention;

FIGS. 6 and 6A depict sections showing electrically conductive plugs in accordance with the invention formed in the substrate of FIGS. 5 and 5A;

FIGS. 7 and 7A depict sections showing an electrically conductive barrier layer and bottom electrode layer deposited in accordance with the invention on the substrate shown in FIGS. 6 and 6A;

FIGS. 8 and 8A depict sections showing a layer of ferroelectric layered superlattice material and a top stack-electrode layer deposited in accordance with the invention on the substrate shown in FIGS. 7 and 7A;

FIGS. 9 and 9A depict sections showing capacitor stacks formed in accordance with the invention by patterning and etching the substrate shown in FIGS. 8 and 8A;

FIGS. 10 and 10A depict sections showing a third insulator layer deposited in accordance with the invention on the substrate shown in FIGS. 9 and 9A;

FIGS. 11 and 11A depict sections in which the third insulator shown in FIGS. 10 and 10A was partially removed in accordance with the invention, thereby exposing a top surface of top stack-electrodes;

FIGS. 12 and 12A depict sections in which a top plate-line electrode layer was deposited in accordance with the invention on the substrate shown in FIGS. 11 and 11A;

FIGS. 13 and 13A depict sections in which portions of the top plate-line electrode layer and other third insulator layer, as shown in FIGS. 12 and 12A, were removed in accordance with the invention, thereby exposing a switch area of the nonconductive buried diffusion barrier layer;

FIGS. 14 and 14A depict sections in which a nonconductive hydrogen barrier layer was deposited in accordance with the invention on the substrate shown in FIGS. 13 and 13A, thereby completely covering a capacitor and a switch in a memory cell;

FIGS. 15 and 15A depict sections in which a fourth insulator layer, electrical connections, and wiring metallization were formed in accordance with the invention on the substrate shown in FIGS. 14 and 14A;

FIG. 16 depicts in schematic form a top view of a horizontal section of the substrate shown in FIGS. 15 and 15A;

FIG. 17 depicts in schematic form a section of an integrated circuit substrate of an alternative embodiment in accordance with the invention, at an early fabrication phase, comprising capacitor stacks covered by a second insulation layer;

FIG. 18 depicts a section of the substrate shown in FIG. 17 after patterning and etching of the substrate and deposition of a top plate-line electrode layer in accordance with the invention;

FIG. 19 depicts a section of the substrate shown in FIG. 18 after etching of portions of the top plate-line electrode layer and the second insulation layer in accordance with the invention; and

FIGS. 20 and 20A depict sections of the substrate shown in FIG. 19 after formation of a nonconductive hydrogen barrier layer and metallization layers in accordance with the invention.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments in accordance with the invention are described herein with reference to FIGS. 1 – 20A. It should be understood that FIGS. 2 – 20A, depicting integrated circuits in sequential stages of fabrication in accordance with the invention, are not meant to be actual plan or cross-sectional views of an actual integrated circuit device. In actual devices, the layers will not be as regular and

the thicknesses may have different proportions. The various layers in actual devices often are curved and possess overlapping edges. The figures instead show idealized representations which are employed to explain more clearly and fully embodiments of the invention than would otherwise be possible. Also, the figures represent only one of innumerable variations of ferroelectric and dielectric devices that could be fabricated in accordance with the invention.

General manufacturing processes for fabricating integrated circuits containing MOSFETs and ferroelectric capacitor elements are described in U.S. Patent No. 5,466,629 issued November 14, 1995 to Mihara et al., and U.S. Patent No. 5,468,684 issued November 21, 1995 to Yoshimori et al., which are hereby incorporated by reference as if fully disclosed herein. General fabrication methods have been described in other references also.

U.S. Patent No. 5,519,234 issued May 21, 1996 to Paz de Araujo et al. is hereby incorporated herein by reference as though fully disclosed herein, and discloses that layered superlattice compounds, such as strontium bismuth tantalate, have excellent properties in ferroelectric applications as compared to the best prior materials and have high dielectric constants and low leakage currents. U.S. Patent No. 5,434,102 issued July 18, 1995, to Watanabe et al. and U.S. Patent No. 5,468,684 issued November 21, 1995, to Yoshimori et al., also both hereby incorporated by reference as though fully disclosed herein, describe processes for integrating these materials into practical integrated circuits.

The layered superlattice materials may be summarized generally under the formula:

$$(1) \quad A1_{w1}^{+a1}A2_{w2}^{+a2}...Aj_{wj}^{+aj}S1_{x1}^{+s1}S2_{x2}^{+S2}...Sk_{xk}^{+sk}B1_{y1}^{+b1}B2_{y2}^{+b2}...Bl_{yl}^{+bl}Q_{z}^{-q}$$

where A1, A2...Aj represent A-site elements in the perovskite-like structure, which may be elements such as strontium, calcium, barium, bismuth, lead, and others; S1, S2...Sk represent superlattice generator elements, which usually is bismuth, but can also be materials such as yttrium, scandium, lanthanum, antimony, chromium, thallium, and other elements with a valence of +3; B1, B2...Bl represent B-site elements in the perovskite-like structure, which may be elements such as titanium, tantalum, hafnium, tungsten, niobium, zirconium, and other elements; and Q represents an anion, which generally is oxygen but may also be other elements,

such as fluorine, chlorine and hybrids of these elements, such as the oxyfluorides, the oxychlorides, etc. The superscripts in formula (1) indicate the valences of the respective elements; for example, if Q is oxygen, then q=2. The subscripts indicate the number of moles of the material in a mole of the compound, or in terms of the unit cell, the number of atoms of the element, on the average, in the unit cell. The subscripts can be integer or fractional. That is, formula (1) includes the cases where the unit cell may vary uniformly throughout the material; for example, in $SrBi_2(Ta_{0.75}Nb_{0.25})_2O_9$, 75% of the B-sites are occupied by strontium atoms, and 25% of the B-sites are occupied by barium atoms. If there is only one A-site element in the compound, then it is represented by the "A1" element and w2...wj all equal zero. If there is only one B-site element in the compound, then it is represented by the "B1" element, and y2...yl all equal zero, and similarly for the superlattice generator elements. The usual case is that there is one A-site element, one superlattice generator element, and one or two B-site elements, although formula (1) is written in the more general form since the invention is intended to include cases where either of the sites and the superlattice generator can have multiple elements. The value of z is found from the equation:

(2) $(a1w1 + a2w2...+ajwj) + (s1x1 + s2x2...+skxk) + (b1y1 + b2y2...+ blyl) = qz.$

Formula (1) includes all three of the Smolenskii type compounds discussed in U.S. Patent No. 5,519,234, referenced above. The layered superlattice materials do not include every material that can be fit into Formula (1), but only those which form crystalline structures with distinct alternating layers.

U.S. Patent No. 5,803,961, issued September 8, 1998 to Azuma et al., which is hereby incorporated herein by reference as though fully disclosed herein, discloses that mixed layered superlattice materials, such as strontium bismuth tantalum niobate, can have even more improved properties in ferroelectric applications. The mixed layered superlattice materials are characterized by nonstoichiometric amounts of A-site and B-site elements. For example, a preferred precursor used in accordance with the invention comprises metal organic precursor compounds having metals in relative molar proportions corresponding to the stoichiometrically unbalanced formula $Sr_{0.8}Bi_2(Ta_{0.7}Nb_{0.3})_2O_{8.8}$.

Currently, ferroelectric layered superlattice materials, like the metal oxides $SrBi_2Ta_2O_9$ (SBT), $SrBi_2(Ta_{1-x}Nb_x)_2O_9$ (SBTN), where $0 \leq x \leq 1$, and particularly $Sr_aBi_b(Ta_{1-x}Nb_x)_cO_{[9+(a-1)+(b-2)(1.5)+(c-2)(2.5)]}$, where $0.8 \leq a \leq 1$, $2 \leq b \leq 2.2$, $0 \leq x \leq 0.3$ and $1.9 \leq c \leq 2.1$ (SBTN), are being used and are under further development for use as capacitor dielectric in nonvolatile memory applications, such as in FeRAMs and nondestructible read-out ferroelectric FETs. Polycrystalline thin films of these layered superlattice materials, as well as other layered superlattice materials represented by Formula (1), may be fabricated and used in accordance with the invention.

The word "substrate" can mean the underlying semiconductor material 204 on which the integrated circuit is formed, as well as any object on which a thin film layer is deposited. In this disclosure, "substrate" shall generally mean the entire workpiece as it exists at a particular phase of fabrication and on which a particular fabrication process is being conducted.

The long dimensions of integrated circuit substrate 202 and semiconductor material 204 in FIGS. 2, 2A – 15A, and 17 – 20A define planes that are considered to be a "horizontal" plane herein, and directions perpendicular to this plane are considered to be "vertical". Terms of orientation herein, such as "above", "top", "upper", "below", "bottom", and "lower", mean relative to semiconductor material 204. That is, if a second element is "above" a first element, it means it is farther from semiconductor material 204; and if it is "below" another element, then it is closer to semiconductor material 204 than the other element. Terms such as "above" and "below" do not, by themselves, signify direct contact. However, terms such as "on" or "onto" do signify direct contact of at least a portion of one layer with at least a portion of an underlying or adjacent layer. As depicted in FIGS. 2 – 20A, a single layer of memory cells comprising switches and capacitors is formed on semiconductor material 204 of an integrated circuit substrate 202. It is understood that embodiments in accordance with the invention also provide a plurality of layers of memory cells formed sequentially one on top of the other on a single integrated circuit substrate.

The term "thin film" is used herein as it is used in the integrated circuit art. Generally, it means a film of less than a micron in thickness. The thin films

disclosed herein are usually less than 500 nanometers (nm) in thickness, and more typically in a range of about from 5 nm to 200 nm. For example, a thin film of layered superlattice material fabricated in an integrated circuit in accordance with the invention typically has a final thickness in a range of from 25 nm to 150 nm. These thin films of the integrated circuit art should not be confused with the layered capacitors of the macroscopic capacitor art which are formed by a wholly different process that is incompatible with the integrated circuit art.

The term "stoichiometric" herein may be applied to both a solid film of a material, such as a layered superlattice material, or to the precursor for forming a material. When it is applied to a solid thin film, it refers to a formula which shows the actual relative amounts of each element in a final solid thin film. When applied to a precursor, it indicates the molar proportion of metals in the precursor. A "balanced" stoichiometric formula is one in which there is just enough of each element to form a complete crystal structure of the material with all sites of the crystal lattice occupied, though in actual practice there always will be some defects in the crystal at room temperature. For example, both $SrBi_2(TaNb)O_9$ and $SrBi_2(Ta_{1.5}Nb_{0.5})O_9$ are balanced stoichiometric formulae. In contrast, a precursor for strontium bismuth tantalum niobate in which the molar proportions of strontium, bismuth, tantalum, and niobium are 0.9, 2.18, 1.5, and 0.5, respectively, is represented herein by the unbalanced "stoichiometric" formula $Sr_{0.9}Bi_{2.18}(Ta_{1.5}Nb_{0.5})O_9$, since it contains excess bismuth and deficient strontium relative to the B-site elements tantalum and niobium. It is common in the art to write an unbalanced stoichiometric formula of a metal oxide in which the subscript of the oxygen symbol is not corrected to balance completely the subscript values of the metals.

The term "strontium tantalate" (or "strontium tantalum oxide") herein means any one or several of the oxide compounds comprising strontium and tantalum. Strontium tantalate in accordance with the invention is represented herein by the generalized stoichiometric formula $SrTaO_x$, which represents strontium tantalate compounds including, but not limited to, $SrTa_2O_6$ and $Sr_2Ta_2O_7$.

The terms "region" and "area" as used herein generally have their usual meaning; that is, “area” generally designates a two-dimensional surface, whereas

a "region" is generally three-dimensional. For example, a "nonmemory area" of a layer or a substrate in this specification generally corresponds to a "nonmemory region" of an integrated circuit located below or above a nonmemory area.

The terms "dielectric thin film", "capacitor dielectric", and similar terms referring to a thin film of dielectric material between electrodes in a capacitor are used broadly to include not only the purely insulating dielectric materials, but also ferroelectric materials that are both dielectric and ferroelectric, such as certain ABO_3-type oxides and, in particular, ferroelectric layered superlattice materials.

The term "continuous" and similar terms used to describe a diffusion barrier layer or a combination of diffusion barriers means substantially unbroken or uninterrupted.

The diagram of FIG. 1 is a flow sheet of a method 100 in accordance with the invention for making a preferred embodiment of a ferroelectric memory in accordance with the invention. Although method 100 of FIG. 1 is discussed herein with reference to FIGS. 2 – 16 representing a ferroelectric memory comprising a thin film of polycrystalline layered superlattice material, it is clear that the method of FIG. 1 and numerous embodiments of a method in accordance with the invention are useful generally for fabricating an integrated circuit that provides protection of one or more elements of the integrated circuit against undesired diffusion of a chemical species to or away from the element.

FIG. 2 depicts in schematic form a section 200 of an integrated circuit substrate 202. In processes 104, a substrate 202 is provided containing silicon semiconductor material 204, field oxide regions 206, and switches 208. A switch 208 is typically a metal-oxide semiconductor field-effect transistor ("MOSFET"), formed using techniques known in the art. A MOSFET switch 208 includes a source region 210, a drain region 212, a channel region 214, gate buffer layer 216, gate insulating layer 218, and gate electrode 220. Substrate 202 further includes a first insulator layer 224, typically called an interlayer dielectric layer ("ILD"), disposed on substrate 202, and covering semiconductor material 204, oxide regions 206, and switches 208. First insulator layer 224 typically comprises nondoped silicate glass ("NSG") or a doped glass, such as BPSG (boron-doped phospho-silicate glass), and is typically formed by reacting a precursor using a

CVD technique as known in the art. In other embodiments in accordance with the invention, integrated circuit substrate 202 comprises gallium arsenide or other semiconductor, or an insulator such as magnesium oxide (MgO).

In processes 106, an electrically nonconductive "buried" diffusion barrier layer 226 is formed on first insulator layer 224, as depicted in FIG. 3, showing section 300. Nonconductive buried diffusion barrier layer 226 preferably comprises silicon nitride, SiN, and typically has a thickness in a range of about from 50 nm to 200 nm, preferably about 100 nm. Silicon nitride is deposited using techniques known in the art, preferably, a CVD or PECVD technique. Silicon nitride is a good diffusion barrier against diffusion of atomic and molecular oxygen and hydrogen, as well as against other chemical species.

In processes 108, as depicted in FIG. 4 showing section 302, a second insulator layer 228a is formed on buried diffusion barrier layer 226, preferably using a CVD process for forming NSG or a doped glass. Second insulator layer 228a typically has a thickness of about 50 nm to 200 nm, preferably about 100 nm.

In processes 110, substrate 202 is patterned and portions of second insulator layer 228, buried diffusion barrier layer 226, and first insulator layer 224 are removed to form vias 230, as depicted in FIGS. 5 and 5A, showing sections 304, 305, respectively. FIG. 5A depicts a cross-section 301 of substrate 202 taken through lines 5A of FIG. 5. In this specification, the horizontal layers depicted in FIG. 5 define a plate-line axis, and the horizontal layers of FIG. 5A define a bit-line axis, which is substantially perpendicular to the plate-line. Patterning is conducted using techniques known in the art, typically photolithographic techniques. Removal of the material is conducted using techniques known in the art, preferably reactive ion etching ("RIE") techniques.

In processes 112, electrically conductive plugs 232 are formed by filling vias 230 with electrically conductive material and planarizing the surface of substrate 202 so that tops 233 of plugs 232 are approximately coplanar with second insulator layer 228a, as depicted in FIGS 6 and 6A showing sections 306, 307, respectively. Plugs 232 are formed so that bottom 234 of each plug 232 is in electrical contact with switch 208. Preferably, conductive plugs 232 comprise tungsten, which is deposited in using techniques known in the art. In more

preferred embodiments, plugs 232 are formed by depositing a layer of titanium having a thickness in a range of about from 5 nm to 30 nm in via 230, followed by depositing a layer of titanium nitride having a thickness in a range of about from 5 nm to 30 nm on the titanium, followed by deposition of tungsten.

In processes 114, electrically conductive oxygen-diffusion barrier layer 236a is deposited on substrate 202, covering second insulator layer 228 and conductive plugs 232, as depicted in FIGS. 7 and 7A, showing sections 308, 309, respectively. In preferred embodiments, electrically conductive oxygen-diffusion barrier layer 236a comprises a laminate structure comprising an iridium oxide sublayer, which is on an iridium sublayer, which is on a titanium aluminum nitride sublayer, as represented by IrO_x/Ir/TiAlN. A preferred laminate stack is fabricated by first sputtering a sublayer of titanium aluminum nitride having a thickness of about 50 nm onto second insulator layer 228a and conductive plugs 232, then sputtering about 100 nm iridium metal onto the nitride sublayer, and then sputtering about 100 nm of iridium oxide onto the iridium sublayer.

In processes 116, bottom electrode layer 238a is formed on conductive diffusion barrier layer 236a, as depicted in FIGS. 7 and 7A. Preferably, bottom electrode layer 238a has a thickness of about 100 nm and comprises platinum. Typically, bottom electrode layer 238a is formed by sputtering a platinum target, using techniques known in the art. Preferably, the electrode is formed by RF sputtering of a platinum single layer, but it also may be formed by DC sputtering, ion beam sputtering, vacuum deposition, or other appropriate conventional deposition process. The bottom and top electrodes of memory capacitors in accordance with the invention preferably contain platinum. Nevertheless, in certain embodiments, a bottom electrode comprises another non-oxidized precious metal, such as palladium, silver, and gold. In addition to the precious metals, a metal such as aluminum, aluminum alloy, aluminum silicon, aluminum nickel, nickel alloy, copper alloy, and aluminum copper may be used to form electrodes of a memory capacitor in accordance with the invention.

In processes 118, metal-oxide capacitor dielectric layer 240a is formed on bottom electrode layer 238a, as depicted in FIGS. 8 and 8A, showing sections 310, 311, respectively. Embodiments in accordance with the invention are particularly

useful for protecting against undesired diffusion in integrated circuits comprising metal-oxide dielectric thin films comprising ferroelectric layered superlattice material. Prior to processes 118 of preferred embodiments, chemical precursors of the desired layered superlattice material are prepared. Usually, precursor solutions are prepared from commercially available solutions containing the chemical precursor compounds. If necessary, the concentrations of the various precursors supplied in the commercial solutions are adjusted to accommodate particular manufacturing or operating conditions. More preferred embodiments in accordance with the invention utilize a final liquid precursor solution containing relative molar proportions of the elements strontium, bismuth, tantalum, and niobium corresponding approximately to $SrBi_2Ta_2O_9$ (SBT), $SrBi_2(Ta_{1-x}Nb_x)_2O_9$ (SBTN), where $0 \leq x \leq 1$, and particularly $Sr_aBi_b(Ta_{1-x}Nb_x)_cO_{[9+(a-1)+(b-2)(1.5)+(c-2)(2.5)]}$, where $0.8 \leq a \leq 1$, $2 \leq b \leq 2.2$, $0 \leq x \leq 0.3$ and $1.9 \leq c \leq 2.1$. Liquid-source metal organic chemical deposition ("LSMCD") and CVD methods for preparing thin films of ferroelectric layered superlattice material have been described in the prior art, including U.S. Patent No. 6,326,315 B1, issued December 4, 2001 to Uchiyama et al., U.S. Patent No. 6,245,580 B1, issued June 12, 2001 to Solayappan et al., and U.S. Patent No. 6,110,531, issued August 29, 2000 to Paz de Araujo et al., which are hereby incorporated by reference. Preferably, processes 118 include a pre-top-electrode RTP treatment ("pre-TE RTP") in accordance with a preferred low-thermal-budget method for forming layered superlattice material.

In processes 120, a top stack-electrode layer 242a is formed on dielectric layer 240a, as depicted in FIGS. 8 and 8A. Top stack-electrode layer 242a preferably has a thickness of about 50 nm and comprises platinum. Typically, a platinum stack-electrode layer 242a is deposited using a sputtering technique, known in the art. Preferably, the electrode is formed by RF sputtering of a platinum single layer, but it also may be formed by DC sputtering, ion beam sputtering, vacuum deposition, or other appropriate conventional deposition process.

In processes 122, a capacitor stack 244 is formed by removing portions of top stack-electrode layer 242a, capacitor dielectric layer 240a, bottom electrode layer 238a, and conductive oxygen-diffusion barrier layer 236a, as depicted in

FIGS. 9 and 9A, respectively. In preferred embodiments, a TEOS hardmask having a thickness of about 300 nm is deposited on top stack-electrode layer 242a using a CVD technique known in the art. Then the TEOS hard mask is patterned using photolithography techniques known in the art, for example, by depositing a resist, then exposing and developing the resist. A full stack etch is then conducted, typically using RIE, to etch the layers down to bottom electrode layer 238a, but not including conductive barrier layer 236a. Then the hard mask is removed using techniques known in the art, and finally barrier layer 236a is etched using RIE to form capacitor stacks 244, each capacitor stack 244 comprising top stack-electrode 242, capacitor dielectric thin film 240, bottom electrode 238, and conductive oxygen-diffusion barrier 236, as depicted in FIGS. 9 and 9A. Conductive oxygen-diffusion barrier 236 is in electrical contact with bottom electrode 238 above, and with conductive plug 232 below. Top stack-electrode 242 has a top surface 246. During later processes described below, a top plate-line electrode is formed, thereby electrically connecting a plurality of capacitor stacks 244. Top stack-electrode layer 242a is formed on metal oxide dielectric thin film layer 240a in order to protect metal oxide dielectric layer 240a against undesired etching during etching of the substrate during processes 122 to form capacitor stack 244. Typically, metal-oxide dielectric layer 240a is thin, preferably in a range of about from 25 nm to 120 nm. Top stack-electrode layer 242a protects metal-oxide dielectric layer 240a against physical and chemical damage during various processes preceding deposition of a top plate-line electrode layer.

In processes 124, a third insulator layer 250a, referred to as the capacitor insulator layer, is formed on integrated circuit substrate 202, in particular on second insulator layer 228 and on capacitor stacks 244, usually completely covering capacitor stacks 244, as depicted in FIGS. 10 and 10A, showing sections 314, 315, respectively. Third insulator layer 250a is typically formed by depositing approximately 500 nm of NSG or doped silicate glass, typically using TEOS or other precursor in a PECVD technique, as known in the art. Then a portion of third insulator layer 250a is completely removed from at least a contact portion of top surface 246 of top stack-electrode 242. In certain embodiments, a portion of third insulator layer 250a is removed by etching through the insulator layer above

capacitor stacks 244 down to top stack-electrode 242, thereby forming a via or contact hole for an electrical contact to a plate-line electrode. In preferred embodiments, third insulator layer 250a is planarized, using a CMP technique as known in the art, to expose top surface 246 of top stack-electrode 242 and form third insulator layer 250b, as depicted in FIGS. 11 and 11A, showing sections 316, 317, respectively. Preferably, third insulator layer 250b is planarized or otherwise shaped so that top 251 of insulator 250b is slightly below top surface 246 of top stack-electrode 242. Nevertheless, top 251 of insulator 250b preferably is not as low as any part of metal oxide dielectric thin film 240.

In processes 126, a top plate-line electrode layer 260a is formed on third insulator layer 250b and top contact surface 246 of top stack-electrode 242 of substrate 202, as depicted in FIGS. 12 and 12A, showing sections 318, 319, respectively. Typically, top plate-line electrode layer 260a is formed by depositing about 150 nm of platinum, using a sputtering technique as known in the art. Preferably, the electrode is formed by RF sputtering of a platinum single layer, but it also may be formed by DC sputtering, ion beam sputtering, vacuum deposition, or other appropriate conventional deposition process. Typically, top plate-line electrode layer 260a is fabricated using material having a composition the same as top stack-electrode 242. In embodiments as depicted in FIGS. 11 and 11A, in which top 251 of insulator 250b is slightly lower than top surface 246 of top stack-electrode 242, top plate-line electrode layer 260a substantially subsumes top stack-electrode 242, as indicated in FIGS. 12 and 12A.

In processes 128, integrated circuit substrate 202 is patterned using a hard mask and photolithography techniques known in the art, and then top plate-line electrode layer 260a and third insulator layer 250b are etched using RIE to form top plate-line electrodes 260 and third insulator layer 250. As depicted in FIGS. 13 and 13A, showing sections 320, 321, respectively, in processes 128, a portion of third insulator layer 250b and a portion of second insulator layer 228a are substantially completely removed above switch area 262 of buried diffusion barrier layer 226, on a bit-line side of capacitor stack 244, adjacent to capacitor portion 264, which corresponds approximately to the footprint of capacitor stack 244; however, portions 263 of layers 250 and 228 adjacent to capacitor stack 244 under

plate line 240 are generally not removed, as depicted in FIG. 13A. Each plate-line electrode 260 defines a plate-line axis, which is perpendicular to the plane of section 320, depicted in FIG. 13, and which is substantially parallel to the plane of section 321 in FIG. 13A. In section 321, depicted in FIG. 13A, a single plate line 260 is shown connecting a plurality of capacitors 270. In preferred embodiments in accordance with the invention, patterning and etching in processes 128 are conducted so that the width of plate-line electrode 260 measured perpendicular to a plate-line axis is wider than capacitor stack 244, as depicted in FIG. 13. As a result, the thin films present in capacitor stacks 244, in particular, the physically and chemically sensitive metal-oxide dielectric thin films 240, are shielded from direct exposure to potentially harmful etching conditions during processes 128. Since third insulator layer 250b is, therefore, not completely etched from protected sidewall 272 of capacitor 270, a thin insulating-oxide layer 274 typically remains on protected sidewall 272. Thus, protected sidewall 272 of capacitors 270 comprises an edge 276 of top plate-line electrode 228, a thin residual layer 274 of insulator oxide, and an edge 278 of second insulator layer 228. Residual insulator oxide layer 274, typically about 10 nm to 40 nm thick, typically covers an edge of conductive diffusion barrier 236, an edge of bottom electrode 238, and an edge of dielectric thin film 240. As depicted in FIG. 13A, portion 263 of third insulator layer 250 is generally not removed adjacent to capacitor stack 244 under plate line 260. Thus, insulated sidewalls 280 of capacitors 270 are covered by third insulator 250. Insulated sidewalls 280 comprise, therefore, side edges, perpendicular to a plate-line axis, of metal-oxide dielectric 240, a bottom electrode 238, and a conductive plug barrier 236.

Generally, in processes 130, a final heating of metal oxide dielectric 240 in oxygen or nonreactive gas is conducted after the etching processes 128 in order to achieve desired electronic properties of polycrystalline metal oxide. In preferred embodiments, capacitor dielectric 240 comprising ferroelectric layered superlattice material has a thickness in a range of about from 25 nm to 300 nm. Preferably, a thin film of ferroelectric layered superlattice material and other elements of a memory capacitor are fabricated using a low-thermal-budget technique. Co-owned and co-pending Untied States Patent Application having the title "Low Thermal

Budget Fabrication Of Ferroelectric Memory Using RTP", filed November date, 2002, which is hereby incorporated by reference, teaches fabrication of thin and ultra-thin films of ferroelectric layered superlattice material in nonvolatile memory capacitors. In an exemplary method, each of a series of 4-inch wafers was processed using MOCVD in a commercially-available AIXTRON Model 1802 CVD apparatus. Each wafer was heated to approximately 170°C and rotated at approximately 10 rpm. The reaction chamber and liquid delivery systems were maintained at a pressure of approximately 6 mbar. The reaction-chamber space was heated to a temperature of about 450°C. Liquid flow streams of approximately 0.2 ccm of each of 0.2 molar SrTa precursor and 0.2 molar bismuth precursor were heated to 200°C in the liquid delivery system and vaporized at 200°C and 6 mbar. Argon carrier gas at a flow rate of approximately 200 ccm carried the vaporized precursors into the reaction chamber into which approximately 1500 ccm of oxygen gas was also flowed. A ferroelectric ("FE") coating was deposited on the bottom electrode substrate at a rate of about 8 nm/min. Then the FE coating on the substrate was pre-TE RTP-treated in accordance with the invention at 650°C for 30 seconds in O_2 gas, with a ramping rate of 100°C per second to form a ferroelectric film. Next, platinum was sputter-deposited on the SBT thin film to make a top electrode layer having a thickness of about 200 nm. The top electrode and SBT layers were milled (dry etch) to form capacitors, and then ashing was performed. Then a post-TE RTP treatment in accordance with a low thermal budget method of the invention was conducted at a hold temperature of 725°C for 2 minutes in O_2 gas. The resulting SBT thin films had a thickness of about 50 nm, and the ferroelectric capacitors had a surface area of 7854 μm^2. Thus, each wafer was heated in the temperature range of about from 650°C to 725°C for a cumulative heating time of only about 150 seconds, or 2½ minutes. No furnace anneal was conducted. A low-thermal-budget technique is usefully applied in accordance with the present invention because, among other effects, the reduced heating time at elevated temperature reduces the formation of hillocks and other non-uniformities at the surfaces of deposited layers. The resulting enhanced smoothness improves interfacial contacts and inhibits electrical shorting.

In processes 132, an electrically nonconductive hydrogen barrier layer 284

is formed on substrate 202 by depositing it on top plate-line electrode 260, protected sidewall 272, and on exposed switch portion 262 of buried diffusion barrier 226, as depicted in FIG. 14. As depicted in FIGS. 14 and 14A, showing sections 322, 323, respectively, nonconductive hydrogen barrier layer 284 completely covers capacitors 270, providing a continuous barrier covering top plate-line electrode 260 along a plate-line axis, and covering protected sidewalls 274 down to buried diffusion barrier 226. Nonconductive hydrogen barrier layer 284 further covers switch region 209 of integrated circuit substrate 202, in particular, switch area 262 on buried diffusion barrier layer 226. Preferably, nonconductive hydrogen barrier 284 comprises strontium tantalum oxide ("strontium tantalate"), having a thickness of about 75 nm. Alternatively, nonconductive hydrogen barrier layer 284 comprises a laminate structure, which laminate structure comprises a sublayer of strontium tantalate, $SrTaO_x$, and a sublayer of silicon nitride, SiN. Preferably, strontium tantalate or a $SrTaO_x$/SiN double-layer is deposited using a MOCVD process and other techniques and structures as described in co-owned and co-pending U.S Patent Application Serial No. 09/998,469, filed November 29, 2001, which is hereby incorporated by reference. Where barrier layer 284 includes only $SrTaO_x$, a 75 nm thick layer of STO is preferably deposited employing MOCVD. Where barrier layer 284 includes both $SrTaO_x$ and SiN, a 75 nm thick sublayer of $SrTaO_x$ is preferably deposited first in a MOCVD process conducted at between 400°C and 600°C, employing a SrTa (strontium tantalum) single source precursor. Thereafter, a layer of SiN, preferably 50 nm to 150 nm thick, is deposited, preferably employing CVD. In an alternative embodiment, the SiN portion of barrier layer 284 may be deposited first, and a layer of $SrTaO_x$ is then deposited on the SiN portion. Liquid spin-on and other liquid-source deposition techniques are also suitable for depositing strontium tantalate in accordance with the invention. Portions of nonconductive hydrogen barrier layer 284 are generally removed from nonmemory areas (discussed below with reference to FIG. 16) of substrate 202 in processes 134. Typically, resist is deposited and patterned using photolithographic techniques, and then an RIE technique is used to etch nonconductive hydrogen barrier layer 284 from nonmemory areas. Both strontium tantalate and silicon nitride, alone or together,

function as oxygen barriers, as well as hydrogen barriers.

In processes 136, as depicted in FIGS. 15 and 15A, showing sections 324, 325, respectively, fourth insulator layer 288 is formed on substrate 202 by depositing approximately 500 nm NSG or doped silicate glass, typically using TEOS or other precursor in a PECVD technique, as known in the art.

In processes 138, a bit-line contact via 290 is etched through insulator layer 288 using techniques known in the art and filled with conductive material, typically tungsten, to form bit-line plug 292, which makes electrical contact with switches 208. Similarly, a plate-line via 294 is etched through insulator layer 288 using techniques known in the art. In certain embodiments in accordance with the invention, via 294 is filled by a tungsten plug 295. In other embodiments, as depicted in FIG. 15A, via 294 is filled by wiring material when wiring layers 296, 297 are deposited during processes 140. Preferably, via 294 and conductive plug 295, or other electrical connection to top plate-line electrode 260, is disposed remotely from capacitors 244 so that the integrity of hydrogen barrier layer 284 is preserved directly above and near capacitors 244. Wiring layers 296, 297 are typically deposited by a conventional Al-Cu-Si metallization sputtering technique.

FIG. 16 depicts in schematic form a top view of a section 400 of substrate 202 taken approximately through lines 16 of FIGS. 15 and 15A. In section 400, memory regions 410, indicated by dashed rectangles, comprise memory capacitors 270 and MOSFET switches 208 (not shown in FIG. 16). Although memory regions 410 are represented in FIG. 16 as having a rectangular shape, it is clear that memory regions 410 in actual integrated circuits have different shapes depending on the particular shapes, locations, and dimensions of capacitors 270 and switches 208. Nonmemory regions of substrate 202 comprise nonmemory regions 411 outside memory regions 410, as represented in FIG. 16. As depicted in FIGS. 15 and 16, a memory region 410 typically comprises at least a portion of conductive bit-line connector plug 292, which provides electrical contact between a switch 208 of a memory cell and a bit-line of an integrated circuit. In preferred embodiments in accordance with the invention, as depicted in FIGS. 15A and 16, conductive plate-line connector plug 295 is disposed remotely from capacitors 270 and memory regions 410. It is a feature of preferred embodiments in accordance

with the invention that nonconductive buried diffusion barrier 226 is disposed throughout an extended area, typically substantially the entire area of an integrated circuit. In other words, buried diffusion barrier 226 is disposed over the extended surface area of FIG. 16 and underlies substantially completely all of the integrated circuit elements depicted in FIG. 16. With reference to FIGS. 15 and 15A, buried diffusion barrier 226 covers virtually all of the surface area of substrate 202 below diffusion barrier 226, with the exception of the areas corresponding to conductive plugs 232, 292. In other words, in preferred embodiments in accordance with the invention, nonconductive buried diffusion barrier 226 is deposited on an extended surface area of the surface of integrated circuit substrate 202 and is not thereafter removed by etching or other means from either active or nonactive regions of the substrate, except to accommodate electrical connections between layers above and below diffusion barrier 226. Also, as depicted in FIGS. 4 – 15A, buried diffusion barrier 226 typically is essentially sandwiched between insulation layer 224 and insulation layer 228 before continued processing of substrate 202.

Buried diffusion barrier 226, preferably comprising silicon nitride, SiN, is both a good hydrogen barrier and a good oxygen barrier. It does not prevent an effective forming-gas anneal of the semiconductor elements in a switch region of a memory cell because sufficient hydrogen or other reducing species diffuses from a reducing ambient through via 290 and through plug 292 to switch region 209 of the substrate, depicted in FIGS. 15 and 15A. Buried diffusion barrier 226 also helps to protect a capacitor 270 against diffusion of hydrogen molecules or other reducing chemical species from switch region 209 into capacitor 270. This is especially important for protecting the capacitor dielectric material, in particular, thin films of ferroelectric layer superlattice material, against hydrogen degradation. Similarly, buried diffusion barrier 226 inhibits the diffusion of oxygen and other oxidizing chemical species into switch region 209 and into other semiconductor material regions from a capacitor 270, from other parts of integrated circuit substrate 202, and from processing ambient. Buried diffusion barrier layer 226 and conductive oxygen-diffusion barrier layer 236 together form a continuous oxygen barrier separating capacitor 270 and integrated circuit elements below capacitor 270, such as switch 208 and plugs 232. Nonconductive hydrogen barrier layer 284 and

conductive oxygen-diffusion barrier 236 form a continuous diffusion barrier between a capacitor 270 and a switch region 209 and other semiconductor material. Therefore, nonconductive hydrogen barrier layer 284 and conductive diffusion barrier 236 together function to prevent hydrogen and other reducing species from diffusing from switch region 209 to capacitor 270. Nonconductive hydrogen barrier layer 284 and conductive diffusion barrier 236 continuously envelop capacitor 270 and, thereby, inhibit diffusion of oxygen and other oxidizing chemical species from capacitor 270, in particular, from capacitor dielectric 240 into conductive plugs 232 and into semiconductor regions, such as switch region 209. In preferred embodiments in accordance with the invention, substrate 202 is "over-etched", meaning that the substrate is etched to a level approximately coplanar or slightly lower than conductive diffusion barrier 236, even completely down to nonconductive buried barrier layer 226, as depicted in FIG. 13. As a result, the combination of nonconductive hydrogen barrier layer 284 and conductive plug barrier 236 presents a virtually continuous diffusion barrier between capacitor 270 and switch 208.

Alternative aspects of embodiments in accordance with the invention are depicted in FIGS. 17 – 20A. FIG. 17 depicts in schematic form a section 501 of an integrated circuit substrate 502 comprising semiconductor material 504, switches 508, and a first insulator layer 524 covering switches 508. Self-aligning capacitors stack 544, each capacitors stack 544 comprising a top stack-electrode 542, capacitors dielectric thin film 540, bottom electrode 538, and conductive diffusion barrier 536, are formed in processes corresponding approximately to 114, 116, 118, 120, 122 of FIG. 1. Conductive oxygen-diffusion barrier 536 is located on a capacitor portion 564 of first insulator layer 524. A portion of conductive diffusion barrier 536 is located on the top of conductive plug 532, which provides electrical contact between conductive oxygen-diffusion barrier 536 and switch 508. A second insulator layer 550a is formed to cover capacitors stack 544 and first insulator layer 524. In contrast to embodiments described with reference to FIGS. 2 – 16, no nonconductive buried diffusion barrier is present in substrate 502. In addition, in fabrication processes corresponding approximately to 110, 112 of FIG. 1, a via 531 and a bit-line plug 533 are formed in first insulator layer 524, and a

connector stack 545 is formed concurrently with capacitors stack 544. As depicted in FIG. 18, showing section 602, second insulator layer 550b is partly removed and planarized, and a plate-line electrode layer 560a is deposited on top surface 551 of second insulator layer 550b and top surface 546, in processes corresponding approximately to 124 – 126 of FIG. 1. As depicted in FIG. 19, showing sections 604, top plate-line electrode 560a and second insulator layer 550b are patterned and etched in processes corresponding to 128 of FIG. 1. In FIG. 19, second insulator layer 550 covers a switch area 532 of first insulator layer 562. Connector stack 545 has been etched down to, or almost down to, the top of bit-line diffusion barrier 539. Plate-line electrode 560 is patterned and etched to be slightly wider than capacitors stack 544. As a result, a residual portion 574 of second insulator layer 550b remains on a sidewall 574 of capacitor 570. Typically, after heating of substrate 502 to achieve desired electronic properties of capacitors dielectric 540, nonconductive hydrogen barrier layer 584 is deposited on substrate 502 in processes corresponding approximately to 132 of FIG. 1. In accordance with the invention, nonconductive hydrogen barrier layer 584 is located on top plate-line electrode 560, on residual portion 574, on sidewall 572 of capacitor 570, and on switch portion 562 of second insulator layer 550, as depicted in FIGS. 20 and 20A, showing sections 606, 607, respectively. As a result, nonconductive hydrogen-diffusion barrier layer 584 and conductive oxygen-diffusion barrier 536 together form a continuous diffusion barrier layer between capacitor 570 and switch 508. In addition, nonconductive hydrogen-diffusion barrier layer 584 and conductive diffusion barrier 536 together continuously envelop capacitor 570, in particular capacitor dialectic 540. Preferably, nonconductive hydrogen barrier layer 584 is removed from nonmemory areas of substrate 502. As depicted in FIG. 20, a via 592 is formed in a third insulator layer 588 down to bit-line diffusion barrier 539, which is in electrical contact with bit-line plug 533. Because via 592 is not as long as corresponding via 290 in the embodiment shown in FIG. 15, typically via 592 can be filled in a single deposition operation with wiring metal 593. Wiring metal 593 is typically deposited by a conventional Al-Cu-Si metallization sputtering technique. Preferably, conductive oxygen-diffusion barrier 536 comprises titanium nitride. More preferably, conductive oxygen-diffusion barrier 536 comprises iridium

oxide disposed on iridium metal, which in turn is disposed on titanium aluminum nitride. Preferably, nonconductive hydrogen barrier layer 584 comprises strontium tantalate.

In addition to the unique barrier layer combinations, a key feature of the invention is the process of formation of the capacitors using the planar structure shown best in FIGS. 8 and 8A. The thin top stacked-electrode layer 242a protects the ferroelectric material 240a during the etch processes that pattern the capacitor, while at the same time saving considerable sputtering time and expense as compared to the prior art. In addition, in comparison to other processes in which the complete top plate-line electrode 260a is formed prior to patterning, delaying formation of the plate-line electrode until after the etching yields a better electrode and allows a more efficient layout than was previously possible.

There has been described novel structures and methods of fabricating integrated circuits for protecting devices and elements against physical damage and degradation of electronic properties arising from undesired diffusion of chemical species from one part of an integrated circuit to another, or from undesired diffusion from a processing atmosphere into a sensitive region of an integrated circuit. In particular, certain embodiments in accordance with the invention protect both a switch and a memory capacitor in a memory cell against damage and degradation arising from undesired diffusion of hydrogen and oxygen within an integrated circuit. An advantage of embodiments in accordance with the invention is that a continuous hydrogen-diffusion barrier covers both switch and capacitor in a memory cell. Another feature is that a combination of diffusion barriers continuously separate one device from another device in an integrated circuit; for example, a combination in accordance with the invention separates a switch from a memory capacitor in a memory cell. Another feature is that a combination of diffusion barriers in accordance with the invention continuously envelops a memory capacitor, thereby preventing undesired diffusion of chemical species out of the capacitor, and also preventing undesired diffusion of chemical species into the capacitor. This is important for protecting the thin film of metal-oxide dielectric material in a memory capacitor, in particular, for protecting a film of ferroelectric layered superlattice material in a nonvolatile memory capacitor. It

should be understood that the particular embodiments shown in the drawings and described within this specification are for purposes of example and should not be construed to limit the invention which will be described in the claims below. Further, it is evident that those skilled in the art may now make numerous uses and modifications of the specific embodiments described, without departing from the inventive concepts. For example, for various layers of the integrated circuit disclosed herein, materials other than those disclosed in preferred embodiments may be employed; thicknesses of the materials disclosed, and alternative materials thereto, other than those disclosed may be used; and material deposition and removal techniques other than those disclosed herein may be used; and all such variations are intended to be included within the scope of the present invention. It is also evident that the processes recited may in some instances be performed in a different order, or equivalent structures and processes may be substituted for the various structures and processes described. Consequently, the invention is to be construed as embracing each and every novel feature and novel combination of features present in and/or possessed by the disclosed compositions and their use in fabrication processes, electronic devices, and electronic device manufacturing methods described. The scope of the invention is indicated by the claims.